Remarks

Reconsideration and reversal of the rejections expressed in the Office Action of October 20, 2005 are respectfully contended in view of the following remarks and the application as amended. The present invention relates generally to the damascene process of fabricating an interconnect structure in an integrated circuit, and more particularly to a method for removing separate via layers, which includes combining the via layers into a single mask.

Claims 1-3 were rejected under 35 U.S.C. §102(b) as being anticipated by Kim, U.S. Patent No. 6,487,712. Kim relates to a method of manufacturing a mask for conductive wirings in a semiconductor device, in which a pattern for a dummy wiring is formed to fabricate the mask by using data values for the conductive wirings, without actually forming the dummy wiring pattern on a mask in forming the dummy wiring pattern between conductive wiring patterns spaced apart at a larger interval from each other during the fabrication of the mask of the semiconductor device. Note that a via/contact photomask, wherein the via/contact photomask further comprises a third via/contact pattern serving for forming at least one third functional via/contact plug in a third dielectric layer, is neither disclosed nor contemplated by Kim, and independent claim 1 has been amended to include such a clarification. Therefore, this rejection is overcome.

Claims 1-3 were rejected under 35 U.S.C. §102(e) as being anticipated by Chang et al. (2003/0044059). Chang et al. disclose automated techniques for identifying dummy/main features on a mask layer. For instance, in a multiple mask layer technique, the definition of a dummy/main feature can be based on connectivity information or functional association information; in a geometry technique, the definition of a dummy/main feature can be based on a feature size, a feature shape, a pattern of features, or a proximity of a feature to a neighboring feature. As noted above relative to Kim, the feature of a via/contact photomask further including a third via/contact pattern serving for forming at least one third functional via/contact plug in a third dielectric layer is also not disclosed or contemplated by Chang et al. Thus, this rejection is overcome as well.

For all of the above reasons, it is respectfully contended that the solicited claims define patentable subject matter. Reconsideration and reversal of the rejections expressed in the Office Action of October 20, 2005 are respectfully submitted. The Examiner is invited to call the undersigned if any questions arise during the course of reconsideration of this matter.

Respectfully submitted,

Date: 1/19/06

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